

wherein the circuit information, floorplan and evaluation indices are associated with each other;

a storing unit for storing the associated circuit information, floorplan and evaluation indices

a second input unit for inputting specifications for modifying the floorplan; and

a processing unit for modifying the floorplan according to the specifications to evaluate the modified floorplan according to the evaluation indices.

15. The information processing system in accordance with claim 14, wherein the evaluation indices includes know-how of a designer who designs a semiconductor integrated circuit.

16. An information processing system, comprising:

an input unit for receiving, from external of said information processing system, circuit information of a module constituting a semiconductor integrated circuit, a floorplan which is allocation information of blocks constituting the module; and evaluation indices for evaluating modifications of the floorplan,

wherein the circuit information, floorplan and evaluation indices are associated with each other;

a storing unit for storing the associated circuit information, floorplan and evaluation indices; and

a processing unit for reading the floorplan stored in the storing unit according to specification information when the specification information for modifying the floorplan is input, generating a plurality of floorplan candidates each being modified

based on the read floorplan and the specification information, evaluating the generated floorplan candidates based on the evaluation indices stored in the storing unit, and selecting one floorplan based on an evaluation result.

17. The information processing system in accordance with claim 16, wherein the evaluation indices includes know-how of a designer who designs a semiconductor integrated circuit.

18. An information processing system used for designing a semiconductor integrated circuit, comprising:

a storing unit for storing circuit information of a module constituting the semiconductor integrated circuit, a floorplan which is allocation information of blocks constituting the module, and evaluation indices for evaluating modifications of the floorplan,

wherein the circuit information, floorplan and evaluation indices are associated with each other; and

an input/output unit for transmitting the associated circuit information, floorplan and evaluation indices from the storing unit.

19. The information processing system in accordance with claim 18, wherein the evaluation indices includes know-how of a designer who designs a semiconductor integrated circuit.

20. An information processing system used for designing a semiconductor integrated circuit, comprising:

a circuit designing apparatus; and

a floorplan modifying apparatus,

wherein the circuit designing apparatus comprises:

a first storing unit for storing circuit information of a module constituting the semiconductor integrated circuit, a floorplan which is allocation information of blocks constituting the module, and evaluation indices for evaluating modifications of the floorplan,

wherein the circuit information, floorplan and evaluation indices are associated with each other; and

a first input/output unit for transmitting the stored circuit information, floorplan and evaluation indices, and

wherein the floorplan modifying apparatus comprises:

an input unit for inputting information for modifying the floorplan,

a second input/output unit for receiving the circuit information, floorplan and evaluation indices transmitted from the circuit designing apparatus,

a second storing unit for storing the circuit information, floorplan and evaluation indices received by the second input/output unit, and

a processing unit for modifying the floorplan according to the information input by the input unit, and for evaluating the modified floorplan based on the evaluation indices.

21. The information processing system in accordance with claim 20, wherein the evaluation indices includes know-how of a designer who designs a semiconductor integrated circuit. --